AMENDMENTS TO THE SPECIFICATION:

Please amend the following paragraph beginning at line 18 on page 1 as follows:

FIG.1B is a timing diagram of clock illustrating the timing operation during the access ~~circle~~ cycle of the central processing unit 104A with the SRAM 106 in accordance with the prior art. The exemplary central processing unit 104A accomplishing with a series of 4 read/write ~~circles~~ cycles signal (RD/WR) is illustrated in conjunction with the reading or writing of the data in the temporary storage 202. The central processing unit 104A could access data at any time from the SRAM 106 without delay due to the SRAM 106 is used only for the central processing unit 104A. Shown in FIG.1B, the central processing unit 104A accomplishes data reading or writing of the SRAM 106 with a series of 4 clock ~~circles~~ cycles of processor 112, on condition that accomplishing the address latch enable signal 110 (ALE). However, it is necessary to have a large capacity SRAM 106 for applying the ASIC 100 to a gigantic or complex system, as a result, ASIC 100 would occupy more area and with more complex manufacturing and higher cost.

Please amend the following paragraph beginning at line 20 on page 6 as follows:

When the central processing unit 201A acquires a data address, in case the address latch enable signal 300 (ALE) changes from low level state into high level state, and directs to the temporary storage 202 according to the data address, the data address is transformed at the moment to one corresponding data address of the temporary data segment 210. Next, the central processing unit 201A begins accomplishing with a series of 4 read/write cycle signal 304 even as it accesses the original temporary storage 202. However, it is possible that the memory chip 21 does not assist the central processing unit 201A to access the temporary data segment 210 for the reason of the temporary is being accessing by other CD drive device (such as necessary circuit 204, etc.). In case of continuously accomplishing the clock signal

of processor, an error operation would happen for the central processing unit 201A may access the data with a series of 4 clock ~~circles~~ cycles of processor 302(T1~T4) (the signal flow shown as a dash line with an arrow).

Please amend the paragraph beginning at line 3 on page 8 as follows:

However, it is possible that other CD drive device (such as necessary circuit 204, etc.) is accessing the memory chip 21 when the central processing unit 201A would like to accessing data from the temporary data segment 210. Therefore, the control chip 20 must wait for the memory chip 21 to accomplish current tasks prior to continuing accessing data, and the suspended time of the clock signal (the period of acknowledgement signal 312) is dependent on the current tasks accomplished by the memory chip 21. The acknowledgement signal is revived to high level state configured for allowing the control chip 20 to access data from temporary data segment 210. Taking FIG.3 as an example, the memory chip 21 accomplishes the current tasks with 4 cycles of memory (DRAM_CLOCK) while the central processing unit 201A just wait for 1.33 cycles (because the ratio of DRAM_CLOCK to μP_CLOCK is 3:1, and 4 cycles of memory equal to 1.33 times ~~circles~~ cycles of μP_CLOCK).

Please amend the paragraph beginning at line 14 on page 8 as follows:

It is noticed that the total operating performance by the central processing unit 201A without reducing dues to the clock ~~circle~~ cycle of the central processing unit 201A is longer than one of the memory chip 21. Moreover, the priority of the central processing unit 201A for accessing data from the memory chip 21 is precedent to others, such as only inferior to the DRAM refresh. Thus, the central processing unit 201A would quickly acquire the necessary data when necessarily accessing the temporary data related to the flow control parameters or the numerical arithmetic. Furthermore, the CD drive in the

preferred embodiment of the present invention could be any optical-electronic system, such as a CD-ROM drive, a CD-RW drive, a DVD-ROM drive, a DVD+R drive, a DVD+RW drive, or a DVD-RAM drive. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.